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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 10

Complete if Known	
Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
DW	AA	US-4,852,098	07/25/1989	Brechard, et al.	
	AB	US-4,875,161	10/17/1989	Lahti, et al.	
	AC	US-4,949,294	08/14/1990	Wambergue, et al.	
	AD	US-4,953,073	08/28/1990	Moussouris, et al.	
	AE	US-4,959,779	09/25/1990	Weber, et al.	
	AF	US-5,081,698	01/14/1992	Kohn	
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	AH	US-5,155,816	10/13/1992	Kohn	
	AI	US-5,161,247	11/03/1992	Murakami, et al.	
	AJ	US-5,179,651	01/12/1993	Taaffe, et al.	
	AK	US-5,231,646	07/27/1993	Heath, et al.	
	AL	US-5,233,690	08/03/1993	Sherlock, et al.	
	AM	US-5,241,636	08/31/1993	Kohn	
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	AO	US-5,487,024	01/23/1996	Girardeau, Jr.	
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	AQ	US-5,533,185	07/02/1996	Lentz, et al.	
	AR	US-5,590,365	12/31/1996	Ide, et al.	
DW	AS	US-5,600,814	02/04/1997	Gahan, et al.	

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DW	AT	WO 93/11500				

Examiner Signature	/Daniel Washburn/	Date Considered	08/18/2006

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Sheet 2 of 10

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
	AU	IEEE Draft Standard for "Scalable Coherent Interface Low-Voltage Differential Signal Specifications and Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018530 – 563)	
	AV	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 – 529)	
	AW	Gerry Kane et al., "MIPS RISC Architecture," Prentice Hall (1995) (50006DOC018576 – 848)	
DW	AX	IBM, "The PowerPC Architecture: A Specification For A New Family of RISC Processors," 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994) (50006DOC019229 – 767)	
	AY	Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set," Manual Part No. 09740-90039, (1990) (50006DOC018849 – 19228)	
	AZ	MIPS Computer Systems, Inc., "MIPS R4000 User's Manual," Mfg. Part No. M8-00040, (1990) (50006DOC017026 – 621)	
	BA	i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn	
	BB	Gove, "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conference, pp. 215-24 (March 1994) (51056DOC000891 – 900)	
	BC	Gove, "The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," IEEE DSP Workshop, pp. 27-30 (October 2-5, 1994) (51056DOC015452 – 455)	
	BD	Guttag et al., "A Single-Chip Multiprocessor for Multimedia: The MVP," IEEE Computer Graphics & Applications, pp. 53-64 (November 1992) (51056DOC000913 – 924)	
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	BM	Lee et al., "Pathlength Reduction Features in the PA-RISC Architecture," IEEE COMPCON, pp. 129-35 (February 24-28, 1992) (51056DOC006816 – 167)	
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Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006

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Sheet 3 of 10

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Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

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DW	BO	US-5,636,351	06/03/1997	Lee	
	BP	US-5,721,892	02/24/1998	Peleg, et al.	
	BQ	US-5,734,874	03/31/1998	Van Hook, et al.	
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DW	BW	US-6,516,406	02/04/2003	Peleg, et al.	

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Sheet 4 of 10

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Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

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DW	BX	Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 – 351)	
DW	BY	Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 – 090)	
	BZ	Hudy et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE Micro, pp. 10-22 (April 1994) (51056DOC002578 – 590)	
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	CP	Abel et al., "Extensions to FORTRAN for Array Processing," ILLIAC IV Document No. 235, Department of Computer Science, University of Illinois at Urbana-Champaign (September 1, 1970) (51056DOC001630 – 646)	
	CQ	Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 – 661)	
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	CS	Awaga et al., "The μVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation," IEEE Micro, Vol. 13, No. 5, pp. 24-36 (October 1993) (51056DOC011921 – 934)	
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Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006

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DW	CU	Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 – 194)	
	CV	Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 – 607)	
	CW	Farnwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291)	
	CX	Farnwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 -034)	
	CY	Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 – 279)	
	CZ	Widdoes, "The S-1 Project: Developing High-Performance Digital Computers," IEEE Computer Society COMPCON Spring 1980 (December 11, 1979) (51056DOC071574 - 585)	
	DA	Correll, S-1 Uniprocessor Architecture SMA-4 (51056DOC056505 - 895)	
	DB	The S-1 Project, January 1985, S-1 Technical Staff (51056DOC057368 – 607)	
	DC	S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 – 918)	
	DD	Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758)	
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	DF	C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157)	
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	DH	Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157)	
	DI	"Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390)	
	DJ	Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993)	
	DK	Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598)	
	DL	Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236)	
	DM	Saturn Overview (November 12, 1993) (51056DOC017111 - 157)	
	DN	Convex Notebook containing various "Machine Descriptions" (51056DOC016994 – 7510)	
	DO	"Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383)	
	DP	Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 – 443)	
	DQ	Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 – 459)	
	DR	Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 – 5299)	
DW	DS	Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394)	

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DW	DT	Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042)	/
	DU	AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392)	—
	DV	Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 – 666)	—
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	DY	Kuhn et al., "A 1,000,000 Transistor Microprocessor," 1989 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 54-55, 290 (February 15, 1989) (51056DOC072091 – 094)	—
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	ED	Mittal et al., "MMX Technology Architecture Overview," Intel Technology Journal Q3 '97, pp. 1-12 (1997) (5156DOC070689 – 700)	/
	EE	Patel et al., "Architectural Features of the i860 – Microprocessor RISC Core and On-Chip Caches," IEEE, pp. 385-90 (1989) (5156DOC070679 – 684)	—
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	EI	i860 XP Microprocessor Data Book, Intel Corporation (May 1991) (51056DOC067266 – 427)	—
	EJ	Paragon User's Guide, Intel Corporation (October 1993) (51056DOC068802 – 9097)	—
	EK	N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982)	—
	EL	N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551)	—
	EM	N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509)	—
	EN	N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441)	—
	EO	N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851)	—
	EP	N12 Performance Analysis document version 2.0, dated September 21, 1990 (51056DOC072992 – 73027)	—
↓	EQ	Hansen, "Architecture of a Broadband Mediaprocessor," IEEE COMPCON 96 (February 25-29, 1996) (MU0013276 – 283 and 51057DOC001825 - 831)	—
DW	ER	Moussouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 – 630)	—

Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	7	of	10

Complete if Known	
Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monc
Attorney Docket Number	43876-144

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
DW	ES	Arnould et al., "The Design of Nectar A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 – 958)	
	ET	Bell, "Ultracomputers: A Teraflop Before Its Time," Communications of the ACM, (August 1992) pp. 27-47 (51056DOC020903 – 923)	
	EU	Broomell et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, pp 95-133 (June 1983) (51056DOC003002 – 040)	
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	EZ	Ghafoor, "Systolic Architecture for Finite Field Exponentiation," IEEE Proceedings, Vol. 136 (November 1989) (51056DOC071700 - 705)	
	FA	Gilot, "Parallel Programming Models and their Interdependence with Parallel Architectures," IEEE Proceedings (September 1993) (51056DOC071792 - 801)	
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	FK	Markstein, "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, pp 111-19 (January 1990) (51056DOC059620 – 628)	
↓	FL	Nienhuis, "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, pp. 1103-05 (1989) (51056DOC061469 – 471)	
DW	FM	Renwick, "Building a Practical HIPPI LAN," IEEE, pp. 355-60 (1992) (51056DOC020937 – 942)	

Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006

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Sheet 8 of 10

Complete if Known	
Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
DW	FN	Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 – 948)	
	FO	Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 – 887)	
	FP	Siegel, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6 (June 1979) (reprinted version pp. 110 118) (51056DOC002949 – 957)	
	FQ	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) (51056DOC020888 – 896)	
	FR	Smith, "Cache Memories," Computing Surveys, Vol. 14, No. 3 (September 1982) (51056DOC071586 - 643)	
	FS	Tenbrink et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science (1994) (51056DOC020943 – 946)	
	FT	Tolmie, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM," Los Alamos National Laboratory Report No. LA-UR 94-3994 (1994) (51056DOC046599 – 609)	
	FU	Tolmie, "HIPPI: It's Not Just for Supercomputers Anymore," Data Communications (May 8, 1995) (51056DOC071802 - 809)	
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	FW	Tullsen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture (June 1995) (51056DOC071434 – 443)	
	FX	Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 – 256)	
	FY	Vetter et al., "Network Supercomputing: Connecting Cray Supercomputers with a HIPPI Network Provides Impressively High Execution Rates," IEEE Network (May 1992) (51056DOC020930 – 936)	
	FZ	Wang, "Bit-Level Systolic Array for Fast Exponentiation in GF(2m)," IEEE Transactions on Computers, Vol. 43, No. 7, pp. 838-41 (July 1994) (51056DOC059407 – 410)	
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DW	GE	Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779)	
	GF	High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801)	
	GG	National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 – 243)	
DW	GH	Wilson, "The History of the Development of Parallel Computing," http://ei.cs.vt.edu/~history/Parallel.html (51056DOC068720 - 757)	

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	First Named Inventor	Craig Hansen
(use as many sheets as necessary)	Group Art Unit	2676
	Examiner Name	Mackly Monestime
Sheet 9 of 10	Attorney Docket Number	43876-144

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DW	GI	IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (51056DOC019304 - 323)	—
		Original Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004	—
	GJ	Amended Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004	—
	GK	Expert Witness Report of Richard A. Killworth, Esq., *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	—
	GL	Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12 2005	—
	GM	Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005	—
	GN	Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005	—
	GO	Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005	—
	GP	Request for *Inter Partes* Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005	—
	GQ	Deposition of Larry Mennemeier on September 22, 2005 and Exhibit 501; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	—
	GR	Deposition of Leslie Kohn on September 22, 2005; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	—
	GS	Intel Article, *"Intel Announces Record Revenue of 9.96 Billion"*, October 18, 2005	—
	GT	The New York Times Article, *"Intel Posts 5% Profit Increase on Demand for Notebook Chips"*, October 19, 2005	—
	GU	USA Today Article, *"Intel's Revenue Grew 18% In Robust Quarter for Tech"*, October 19, 2005	—
	GV	The Wall Street Journal Article, *"Intel Says Chip Demand May Slow"*, October 19, 2005	—
DW	GW	The New York Times Article, *"Intel Settlement Revives A Fading Chip Designer"*, October 20, 2005	—

Examiner Signature	/Daniel Washburn/	Dated Considered	08/18/2006

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SHEET 10 OF 10

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 043876-0144	SERIAL NO. 10/616,303
	APPLICANT Craig HANSEN, et al.	
	FILING DATE July 10, 2003	GROUP 2676

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Codes		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
DW	A	US	6,643,765	11-04-2003	Hansen et al.	
DW	B	US	6,725,356	04-20-2004	Hansen et al.	
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
DW	C	MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005)	
DW	D	Intel Press Release, "Intel Announces Record Revenue of $9.88 Billion," Santa Clara, CA, 10-18-2005	

EXAMINER	DATE CONSIDERED
/Daniel Washburn/	08/18/2006

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